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NOTICE OF ALLOWANCE AND FEE(S) DUE

30425 7590 04/03/2008

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
DAY, HERNG DER	
ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 04/03/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,621	06/09/2000	Vidyabhusan Gupta	99-B-186	3053

TITLE OF INVENTION: SYSTEM AND METHOD FOR DESIGNING AND OPTIMIZING THE MEMORY OF AN EMBEDDED PROCESSING SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1440	$0	$0	$1440	07/03/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,621	06/09/2000	Vidyabhusan Gupta	99-B-186	3053

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nonprovisional	NO	$1440	$0	$0	$1440	07/03/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
DAY, HERNG DER	2128	703-014000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1_____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2_____ 3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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2128	

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 303 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 303 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	09/591,621	GUPTA, VIDYABHUSAN	
	Examiner	Art Unit	
	HERNG-DER DAY	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment received 12/17/07 and RCE received 2/26/08*.

2. ☒ The allowed claim(s) is/are *1-5, 8-12, 22-26, and 29, now renumbered as 1-16*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This communication is in response to Applicant's Amendment and Response to Office Action dated October 15, 2007, filed December 17, 2007, Applicant's RCE to Office Action dated January 22, 2008, filed February 26, 2008, and telephone interview conducted March 28, 2008.

1-1. Claims 1-4, 8-12, and 22-26 have been amended. Claims 6-7, 13-21, and 27-28 have been canceled. Claims 1-5, 8-12, 22-26, and 29 are pending.

1-2. Claims 1-5, 8-12, 22-26, and 29 have been examined and allowed.

EXAMINER'S AMENDMENT

2. An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to Applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this Examiner's amendment was given in a telephone interview with Mr. Daniel E. Venglarik (Reg. No.: 39,409) on March 28, 2008.

4. The claims have been amended as follows:

4-1. Replace claim 1 as follows:

1. (Currently Amended) An apparatus for designing a memory configuration for use in an embedded processing system, the apparatus comprising:

a processing system, the processing system comprising:

a data processor;

a simulation controller ~~capable of~~ simulating execution of a program to be executed by said embedded processing system;

a memory access monitor ~~capable of~~ monitoring~~, during said simulated execution of said program,~~ memory accesses to a simulated memory space during said simulated execution of said program~~, wherein said memory access monitor is capable of~~ and concurrently generating memory usage statistical data associated with said monitored memory accesses, and wherein said memory accesses comprise read operations and write operations; and

a memory optimization controller ~~capable of~~ using said memory usage statistical data, a memory model, and one or more design criteria associated with said embedded processing system ~~to determine at least one~~ determining a plurality of memory configurations ~~capable of~~ satisfying said one or more design criteria and determining a figure of merit for each determined memory configuration, wherein said memory model includes, for each of a plurality of memory types, one or more characteristics selected from write power, refresh power, read power, area per bit, area efficiency, write speed, read speed, erase capability and block size, wherein the figure of merit for each memory configuration indicates a degree to which the respective one of the memory configurations satisfies the one or more design criteria, and wherein said one or more design criteria are selected from memory type usage constraints, memory type size constraints, memory power consumption objectives, and memory speed objectives,

wherein the memory optimization controller selecting one of the determined memory configurations for use in the embedded processing system to best meet the one or more design criteria; and

a code optimization controller automatically modifying the program in response to the memory usage statistical data, the selected memory configuration, and the figure of merit for the selected memory configuration to achieve greater efficiencies.

4-2. Replace claim 2 as follows:

2. (Currently Amended) The apparatus as set forth in Claim 1 wherein ~~said at least one~~ each determined memory configuration is determined from a set of memory types, said set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM).

4-3. Replace claim 3 as follows:

3. (Currently Amended) The apparatus as set forth in Claim 2 wherein ~~said at least one~~ each determined memory configuration comprises a first memory type and a first memory size associated with said first memory type.

4-4. Replace claim 4 as follows:

4. (Currently Amended) The apparatus as set forth in Claim 3 wherein ~~said at least one~~ each determined memory configuration further comprises a second memory type and a second memory size associated with said second memory type.

4-5. Cancel claims 6-7.

4-6. Replace claim 8 as follows:

8. (Currently Amended) A method of designing a memory configuration for use in an embedded processing system, the method comprising the steps of:

simulating execution of a program to be executed by the embedded processing system;

~~monitoring,~~ during the simulated execution of the program, monitoring memory accesses to a simulated memory space, wherein said memory accesses comprise read operations and write operations[[;]], and generating memory usage statistical data associated with the monitored memory accesses;

using the memory usage statistical data, a memory model and one or more design criteria associated with the embedded processing system ~~to determine at least one~~ determining a plurality of memory configurations ~~capable of~~ satisfying the one or more design criteria and determining a figure of merit for each determined memory configuration,

wherein the memory model includes, for each of a plurality of memory types, one or more characteristics selected from write power, refresh power, read power, area per bit, area efficiency, write speed, read speed, erase capability and block size, wherein the figure of merit for each determined memory configuration indicates a degree to which the respective one of the determined memory configurations satisfies the one or more design criteria, and wherein the one or more design criteria are selected from memory type usage constraints, memory type size constraints, memory power consumption objectives, and memory speed objectives;

selecting one of the determined memory configurations for use in the embedded processing system to best meet the one or more design criteria; and

automatically modifying the program in response to the memory usage statistical data, the selected memory configuration, and the figure of merit for the selected memory configuration to achieve greater efficiencies.

4-7. Replace claim 9 as follows:

9. (Currently Amended) The method as set forth in Claim 8 wherein ~~the at least one~~ each determined memory configuration is determined from a set of memory types, the set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM).

4-8. Replace claim 10 as follows:

10. (Currently Amended) The method as set forth in Claim 9 wherein ~~the at least one~~ each determined memory configuration comprises a first memory type and a first memory size associated with the first memory type.

4-9. Replace claim 11 as follows:

11. (Currently Amended) The method as set forth in Claim 10 wherein ~~the at least one~~ each determined memory configuration further comprises a second memory type and a second memory size associated with the second memory type.

4-10. Replace claim 12 as follows:

12. (Currently Amended) The method as set forth in Claim 8 wherein ~~the step of~~ simulating execution of the program comprises ~~the sub-steps of~~ simulating execution of the program N times, wherein ~~the step of~~ monitoring the memory accesses comprises ~~the sub-steps of~~ monitoring the memory accesses during the N simulated executions of the program, and wherein ~~the step of~~ generating the memory usage statistical data is based on the N simulated executions of the program.

4-11. Cancel claims 13-21.

4-12. Replace claim 22 as follows:

22. (Currently Amended) For use in a processing system, a computer-readable storage medium containing computer-executable instructions for designing a memory configuration for use in an embedded processing system, the computer-executable instructions comprising the steps of:

simulating execution of a program to be executed by the embedded processing system;

~~monitoring,~~ during the simulated execution of the program, monitoring memory accesses to a simulated memory space, wherein said memory accesses comprise read operations and write operations[[;]], and generating memory usage statistical data associated with the monitored memory accesses;

using the memory usage statistical data, a memory model and one or more design criteria associated with the embedded processing system ~~to determine at least one~~ determining a plurality of memory configurations ~~capable of~~ satisfying the one or more design criteria and determining a figure of merit for each determined memory configuration, wherein the memory model includes, for each of a plurality of memory types, one or more characteristics selected from write power, refresh power, read power, area per bit, area efficiency, write speed, read speed, erase capability and block size, wherein the figure of merit for each memory configuration indicates a degree to which the respective one of the memory configurations satisfies the one or more design criteria, and wherein the one or more design criteria are selected from memory type usage constraints, memory type size constraints, memory power consumption objectives, and memory speed objectives;

selecting one of the determined memory configurations for use in the embedded processing system to best meet the one or more design criteria; and

automatically modifying the program in response to the memory usage statistical data, the selected memory configuration, and the figure of merit for the selected memory configuration to achieve greater efficiencies.

4-13. Replace claim 23 as follows:

23. (Currently Amended) The computer-readable storage medium as set forth in Claim 22 wherein ~~the at least one~~ each determined memory configuration is determined from a set of memory types, the set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM).

4-14. Replace claim 24 as follows:

24. (Currently Amended) The computer-readable storage medium as set forth in Claim 23 wherein ~~the at least one~~ each determined memory configuration comprises a first memory type and a first memory size associated with the first memory type.

4-15. Replace claim 25 as follows:

25. (Currently Amended) The computer-readable storage medium as set forth in Claim 24 wherein ~~the at least one~~ each determined memory configuration further comprises a second memory type and a second memory size associated with the second memory type.

4-16. Replace claim 26 as follows:

26. (Currently Amended) The computer-readable storage medium as set forth in Claim 22 wherein ~~the step of~~ simulating execution of the program comprises ~~the sub-steps of~~ simulating execution of the program N times, wherein ~~the step of~~ monitoring the memory accesses comprises ~~the sub-steps of~~ monitoring the memory accesses during the N simulated executions

of the program, and wherein ~~the step of~~ generating the memory usage statistical data is based on the N simulated executions of the program.

4-17. Cancel claims 27-28.

Reasons for Allowance

5. The following is an Examiner's statement of reasons for allowance:

5-1. The closest prior art of record discloses:

(1) A software package (Csim) to analyze the structure and behavior of a cache memory and to help the student in the design of cache memories for embedded systems (Giorgi et al., "An Educational Environment for Program Behavior Analysis and Cache Memory Design").

(2) A methodology for developing memory models of on-chip SRAM memory organizations using weighted stepwise linear regression (Coumeri et al., "Memory Modeling for System Synthesis").

(3) A technique allowing runtime selection of statistics gathering, memory profiling, and cache simulation with low overhead (Magnusson et al., "Efficient Memory Simulation in SimICS").

5-2. The prior art does not expressly teach or render obvious the invention as recited in independent claims 1, 8, and 22.

Regarding independent claim 8, the prior art of record, while disclosing developing memory models of on-chip SRAM memory and helping the design of cache memories for embedded systems, does not disclose the distinct combination of features of "during the simulated execution of the program, monitoring memory accesses to a simulated memory space,

… and generating memory usage statistical data associated with the monitored memory accesses", "using the memory usage statistical data, a memory model and one or more design criteria associated with the embedded processing system determining a plurality of memory configurations satisfying the one or more design criteria and determining a figure of merit for each determined memory configuration", and "modifying the program in response to the memory usage statistical data, the selected memory configuration, and the figure of merit for the selected memory configuration to achieve greater efficiencies" as expressly claimed and shown in Fig. 3. Independent claims 1 and 22 include equivalent method limitations as in claim 8.

As stated in MPEP § 2131.02, "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Therefore, the prior art of record does not anticipate, render obvious or read on each independent claim and each independent claim does not read on the prior art.

Dependent claims are allowed as they depend upon the allowable independent claims.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Herng-der Day/
Examiner, Art Unit 2128

March 28, 2008

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128